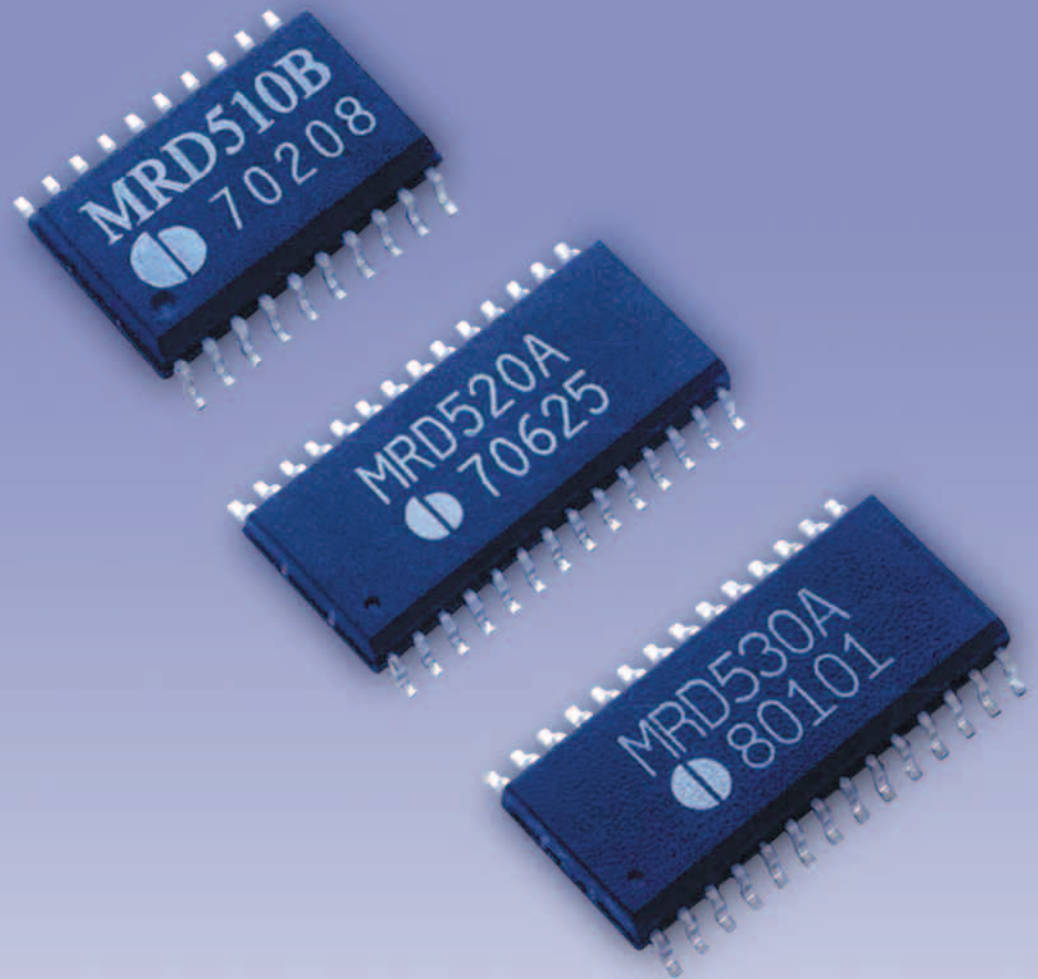


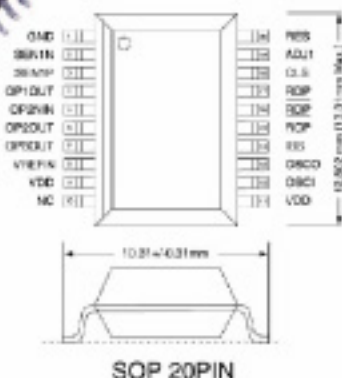
F2F Decoder ASIC IC (TTL Output)



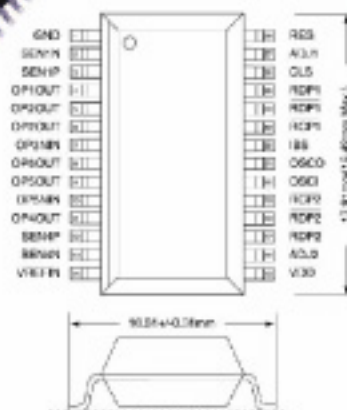
MRD500 Series

- Decoder IC for F2F encoded magnetic stripe
- CMOS integrated circuit with built-in operational amplification circuitry
- Available for single, dual or triple track decoding solutions
- Support 75/210 BPI recording density
- Adjustable output clock pulse width 14 to 60 μ s.
- Ignore start bit selectable for 4 or 8 bits
- Idle mode controllable by external hardware or Micro-Processor
- Accept magnetic head data input frequency from 300 to 12600 bit/sec

F2F Decoder ASIC IC (TTL Output)



SOP 20PIN



SOP 26PIN



SOP 28PIN

Maximum Ratings

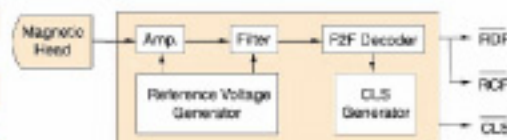
Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply Voltage	VDD	-0.5 to +7.0	V
VIN1	Input Voltage	IBS, OSC1, RES, ADJ1, ADJ2	-0.5 to VCC +0.5	V
VIN2	Input Voltage	OP2IN, OP5IN	-0.5 to VCC +0.5	V
IO	Output Current	OP1OUT, OP2OUT, OP3OUT, OP4OUT, OP5OUT, OP6OUT, OSC2, OUT2, OUT2X, OUT1, OUT1X, OCK1, OCK2	-10 to +10	mA
VID	Differential Input Voltage	SEN1P-SEN1N, SEN2P-SEN2N	-1.0 to +1.0	V
TOPR	Operating Temperature		-30 to +70	°C
TSTG	Storage Temperature		-50 to +140	°C

Recommended Operating Conditions

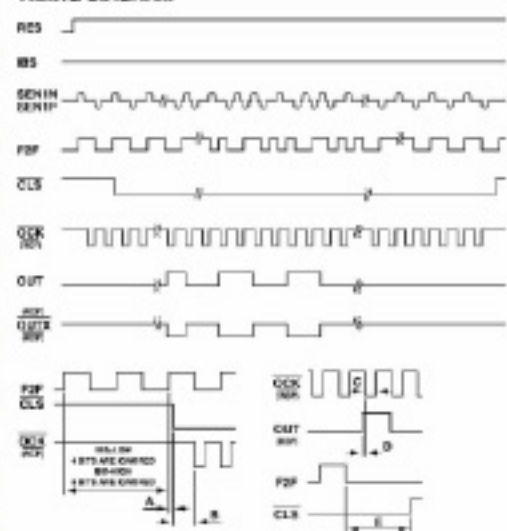
Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
VCC	Supply Voltage		4.5	5	5.5	V
VIH	Input High Voltage	IBS, RES	VCC-0.5		VCC+0.5	V
VIL	Input Low Voltage	IBS, RES	-0.5	0	0.5	V
IOH	Output High Source Current at VOH=VCC-0.4	OCK1, OUT1, OUT1X, OCK2, OUT2, OUT2X	-1.5			mA
IOH	Output High Source Current at VOH=VCC-0.4	CLS	-0.1			mA
IOL	Output Low Sink Current at VOL=0.4	OCK1, OUT1, OUT1X, OCK2, OUT2, OUT2X, CLS	3			mA
VIN	Differential Input Voltage	SEN1P-SEN1N, SEN2P-SEN2N	5		80	mV
FIN	Input Frequency	SEN1P-SEN1N, SEN2P-SEN2N	300		13000	Hz
FOSC	Oscillation Frequency			2.3		MHz
ROSC	External resistor between OSC1 & OSC2			30		Kohm
IOPR	Signal Input at 12.6k bps			3.4	4.0	mA
ISBY	No signal input			2.5	3.0	mA
IDLE	Reset = Vss			1.6	2.0	mA

Model Configuration

Model	Channel	Packing
MRD510	Single	SOP20
MRD520	Dual	SOP26
MRD530	Triple	SOP28



TIMING DIAGRAM



TIME WIDTH OF THE A, B, C, D, E:

- A. APPROXIMATE 2.5US
- B. DINE DATA BIT
- C. ADJUST ADJ1 & ADJ2 PULL HIGH RESISTOR COULD BE ADJUSTED FROM 14US TO 50US
- D. APPROXIMATE 13US
- E. APPROXIMATE 12.5MS AT OSC 2.3MHZ

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