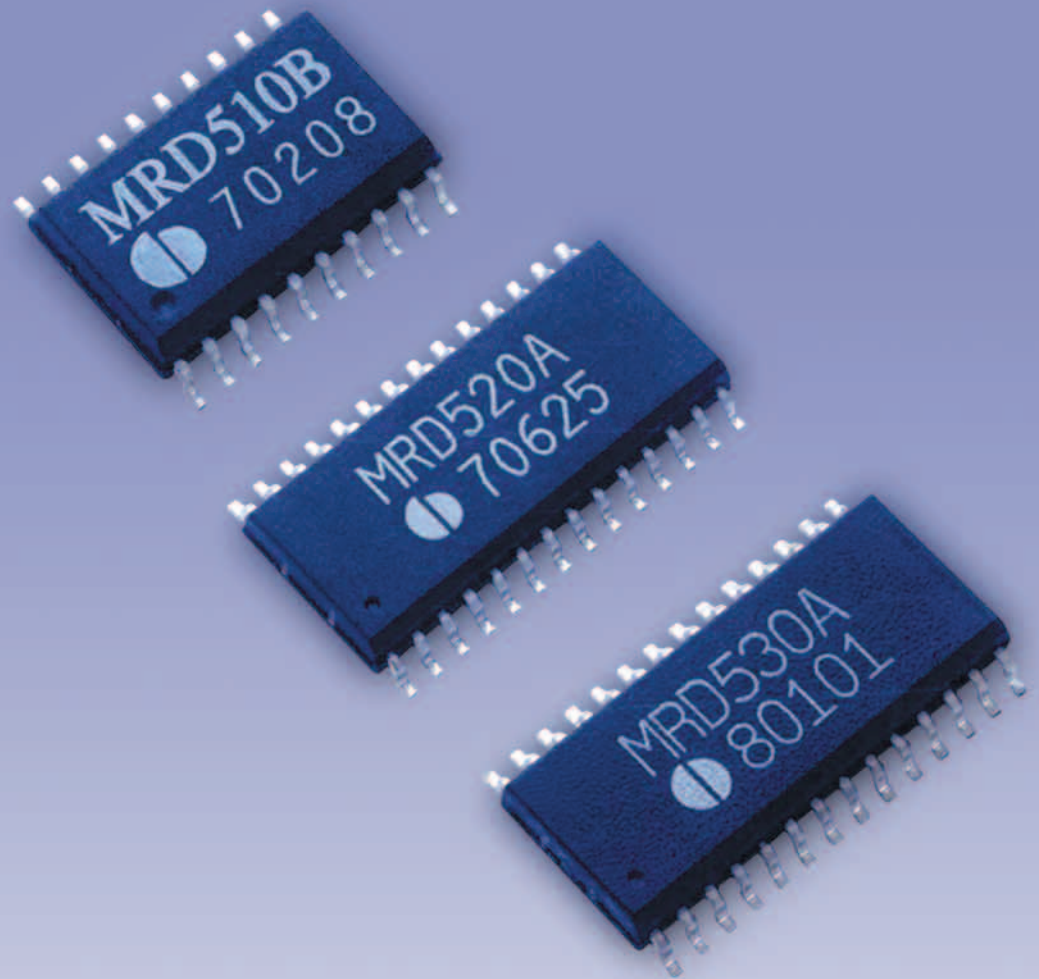


# F2F Decoder ASIC IC (TTL Output)



## MRD500 Series

- Decoder IC for F2F encoded magnetic stripe
- CMOS integrated circuit with built-in operational amplification circuitry
- Available for single, dual or triple track decoding solutions
- Support 75/210 BPI recording density
- Adjustable output clock pulse width 14 to 60  $\mu$ s.
- Ignore start bit selectable for 4 or 8 bits
- Idle mode controllable by external hardware or Micro-Processor
- Accept magnetic head data input frequency from 300 to 12600 bit/sec

